TP44200NM-DPT-EVB

Switching Test Evaluation Board

For

Tagore Technology's GaN FET (TP44200NM)

User Manual

Rev-1.1

2023-September-25

powergan@tagoretech.com

Contents

1 Introduction

This Double Pulse Test (DPT) Evaluation Board (EVB) TP44200NM-DPT-EVB provides users the platform to evaluate the switching behavior of Tagore Technology's "GaN FET with monolithically integrated driver" parts. This document should be used as a user guide only by professionals with adequate technical knowledge. TP44200NM-DPT-EVB can be used to measure switching energy loss, turn-on, and turn-off time.

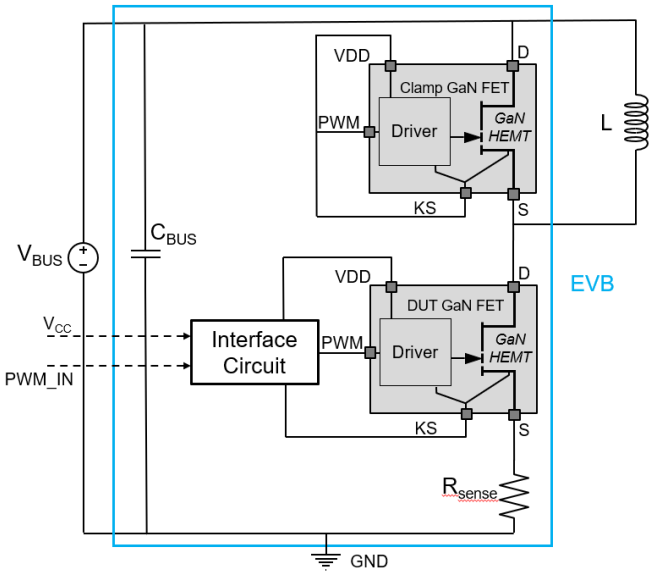

Figure 1-1: Simplified Circuit Diagram of Double Pulse Test Setup.

Figure 1-1 shows a simplified schematic of the Double Pulse Test setup using the TP44200NM-DPT-EVB. Tagore Technology's "GaN FET with monolithically integrated driver" part, TP44200NM is shown as the Device Under Test (DUT). The test setup is fed from a HV DC power source whose voltage is denoted by V_{BUS}. An inductor of inductance L is connected between the drain of the DUT and the positive terminal of V_{BUS}. This inductor is not part of the EVB. When DUT turns on, current will flow from V_{BUS} to the DUT through the inductor. Another TP44200NM acts as the clamp diode. It helps freewheel the inductor current whenever the DUT turns off. The interface circuit adjusts bias voltage for the driver and the input signal (PWM_IN) for the gate, as per the requirement of the DUT. A set of DC bus capacitors (combination of Al-electrolytic and ceramic capacitors, lumped as C_{BUS}) is connected between the input terminals of V_{BUS} to limit voltage fluctuations. Control signal PWM_IN, having two pulses (as shown in Figure 1-2), is fed to the DUT to turn it ON and OFF. When DUT turns ON, the inductor current will flow through the DUT.

Pulse #1 of duration t1 will determine the switching test current I_{SW} of the DUT as the inductor current I_L builds up from 0 to I_{SW} during this pulse. It remains almost constant at I_{SW} during the period t2 in between two pulses. It again starts increasing during the Pulse #2 with a duration of t3. The Turn-on and Turn-off switching transitions can be captured in DSO during the rising edge of PWM pulse #2, and falling edge of PWM pulse #1, respectively.

The rise in inductor current ΔI_L during pulse duration of t_n is given by the following equation:

$$\Delta I_L = \frac{V_{BUS}}{L} \cdot t_n$$

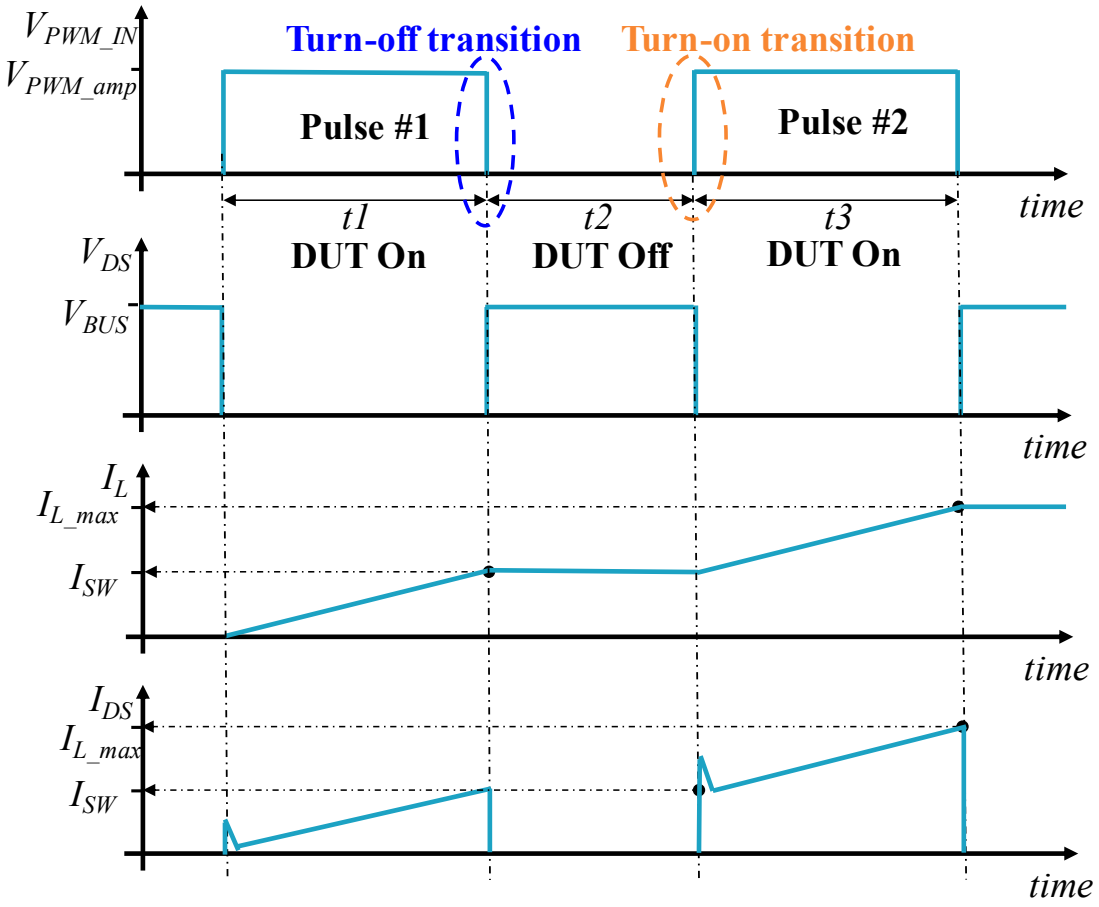

Figure 1-2: Timing Diagram of Double Pulse Test.

Users should be careful while selecting the pulse durations t1 and t3 as these time periods will determine the DUT currents for any given V_{BUS} and L. It is recommended that before performing the actual DPT, the user should calculate the estimated values of t1, t2 and t3 based on the required current settings and V_{BUS} and L values. The duration of t2 should not be too long to ensure that the inductor current stays nearly constant during this freewheeling period. Typically, t2 should be less than 1 µs. The maximum Inductor and DUT current I_{L_max} should be within the recommended maximum pulsed current value mentioned in the datasheet of the DUT. The inductor should be chosen appropriately so that it can carry this current without getting saturated.

2 Physical Details Of EVB

Photographs of both the top and bottom sides of the TP44200NM-DPT-EVB are shown in Figure 2-1 with key components and test points identified.

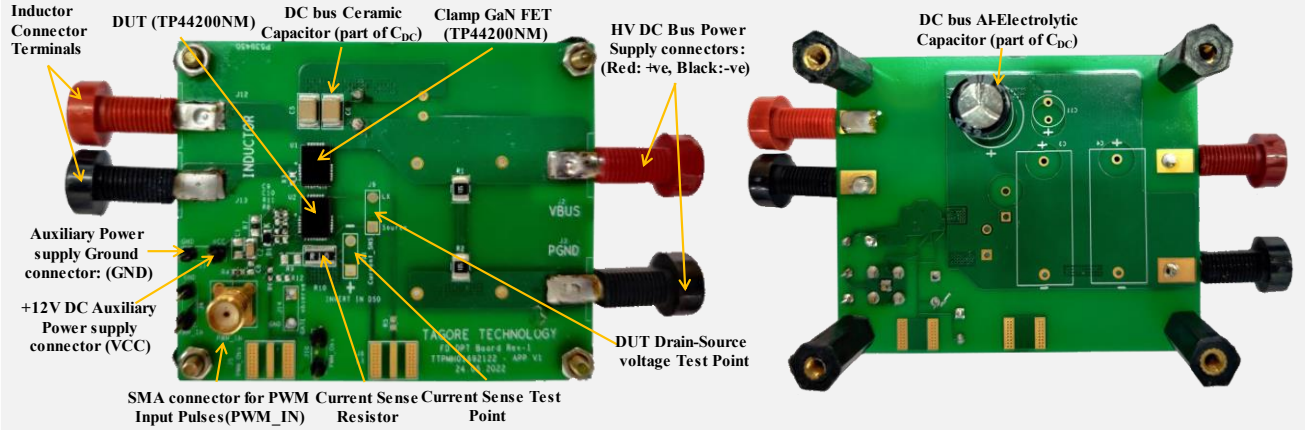

Figure 2-1: Photographs of TP44200NM-DPT-EVB with key components and test points identified. Top View (left); Bottom View (right).

2.1 Dimension Measurements

Table 2-1 : Mechanical Dimensions

Mechanical Dimensions	Value	Unit
Length of EVB PCB	72.19	mm
Width of EVB PCB	59.16	mm
Thickness of PCB	1.6	mm
Height of tallest component on Top Side	12	mm
Height of tallest component on Bottom Side	21	mm

2.2 Technical Data

Table 2-2 : Electrical Parameter Ratings

Parameter	Symbol	Value	Unit	Comments
High Voltage (DC) Input	VBUS	400	V	Maximum
Auxiliary DC Power Supply Voltage	VCC_IN	12	V	0.2 A min. current rating
Amplitude voltage of input PWM pulse	PWM_IN	6	V	Maximum
		5	V	Minimum
Maximum Drain-Source current of DUT	I_{L_max}	**	A	Please check datasheet of DUT

**Check the latest datasheet to get the Maximum Drain-Source current of DUT. Recommended value should not be exceeded.

3 Operating Procedure

3.1 List Of Instruments and Hardware Items Required

For DPT the following list of instruments and hardware items are required:

- TP44200NM-DPT-EVB eval board
- Inductor (preferably with shielding and low parasitic capacitance for cleaner waveforms)
- Controllable PWM signal source (preferably a DSP with 5V amplitude output)
- Power Sources:
  - Auxiliary power source: 12 V DC, 200mA (min)
  - High Voltage power source: 400V DC (max)
- Observation Instruments:
  - Digital Storage Oscilloscope (*abr.* DSO) (Preferably with 4 Channels, BW ≥ 300 MHz)
  - High Voltage Probe (min. 500 V and preferably with spring ground lead) compatible with the DSO
  - Low Voltage Probe/Active Probe compatible with the DSO
  - Current Probe for observing Inductor current (optional)
- Wires and cables for making electrical connections.

3.2 Operating Procedure Steps

- **Step 1:** Connect an inductor in between the connectors J12 and J13 on the TP44200NM-DPT-EVB. Typically, the recommended value of the inductor is in the range of 50 µH to 100 µH.
- **Step 2:** Connect output from a controllable PWM signal source to either SMA connector J6 or header J4.
- **Step 3:** Connect output terminals of an Auxiliary 12 V DC source to the 2-pin header connector J1, to supply power to the interface circuit.
- **Step 4:** To observe the PWM input signal going into the DUT, connect a low-voltage probe from DSO to header connector J10.
- **Step 5:** To observe the Drain-Source voltage signal of the DUT, connect a high-voltage probe from DSO, at connector J9. More details on the probe connection are given in Section 3.3.
- **Step 6:** To observe the Drain-Source current signal of the DUT, connect an Active probe or a low voltage probe from DSO, at connector J11 and invert the signal in DSO. However, this step can be skipped if available DSO channels are limited. More details on the probe connection are given in Section 3.4.
- **Step 7: (Optional)** Connect current probe to any lead wire of the inductor.
- **Step 8:** Turn on the 12 V DC source output with a current limit of 200mA, and then turn on the HV DC source output. It is recommended to first check the test setup at low voltage (preferably less than 30 V). Then release a test pulse signal from the PWM signal generator and observe the waveforms in DSO.
- **Step 9:** If the test setup is ok, then gradually increase the HV DC source output to the desired value up to 400 V. Adjust the PWM pulse widths to get the desired DUT current (limit the peak current to the recommended values as per datasheet of the DUT), and then release the Double Pulse signal from PWM signal generator.

Note that the EVB is designed for the Double Pulse Test only. Make sure there is at least 100 ms rest period (no current period) available between two consecutive sets of pulses (in case of continuous operation) to provide sufficient cooling time for the DUT as there is no heatsink attached to it.

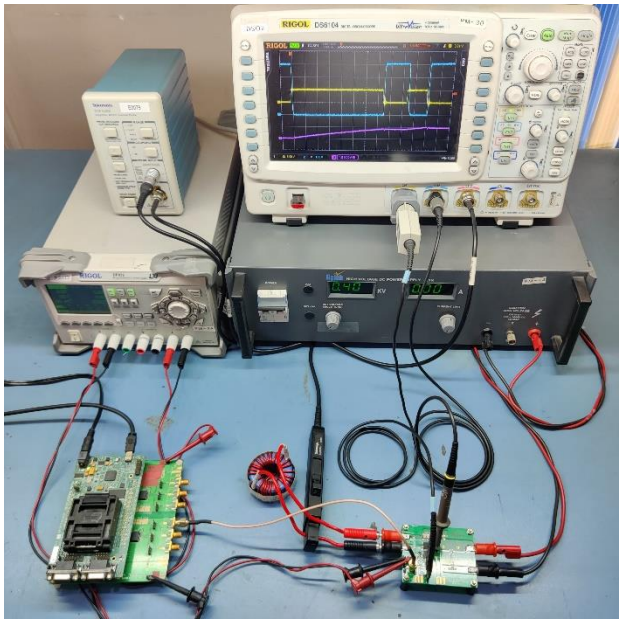

Figure 3-1: Typical Lab Test Setup for DPT.

3.3 Recommended Probe Connection to Observe DUT Drain-Source Voltage

For observing Drain-Source voltage waveform of DUT, the user can connect a voltage probe across the test point J9 with ground lead connected to the “Source” terminal and probe tip connected to the terminal marked as “LX”.

Figure 3-2: Recommended HV probe connection for observing Drain-Source voltage (Left image). Voltage probe with Spring Type Ground lead identified (Right image).

It is recommended to use spring lead for the ground connection of the voltage probe as shown in Figure 3-2. This will help in reducing noise in the waveform observed through DSO. The user should check and ensure that the voltage rating of the probe is higher than the applied HV DC bus voltage while testing the EVB.

3.4 Recommended Probe Connection to Observe DUT Drain-Source Current

For observing Drain-Source current waveform of DUT, the user can probe the voltage across the 0.1Ω current sense resistor on the EVB through test point J11. The tip of the voltage probe should be inserted in the terminal marked by a (+) sign. This will ensure that the voltage probe connection is referred to the 'Source' node of the DUT. Invert this voltage probe signal in DSO to observe current flow from Drain to Source in correct polarity. It is recommended to use an Active probe as shown in Figure 3-3. This will help in reducing noise in the waveform observed through DSO. Alternatively, a low-voltage probe with spring-type ground lead can also be used to observe current waveform with better noise immunity.

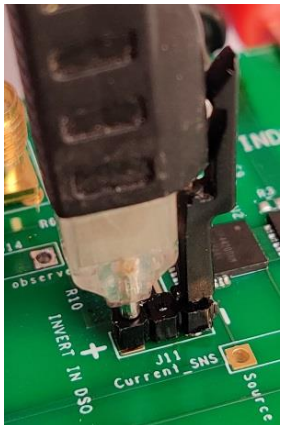

Figure 3-3: Active probe connection for observing Drain-Source Current through current sense

The current value in Ampere will be ten times (10X) that of the voltage measured in Volts since the current sense resistor is 0.1Ω. For example, 100 mV across the current sense resistor corresponds to 1 A Drain-Source current.

4 Key Switching Waveforms Observed From DSO

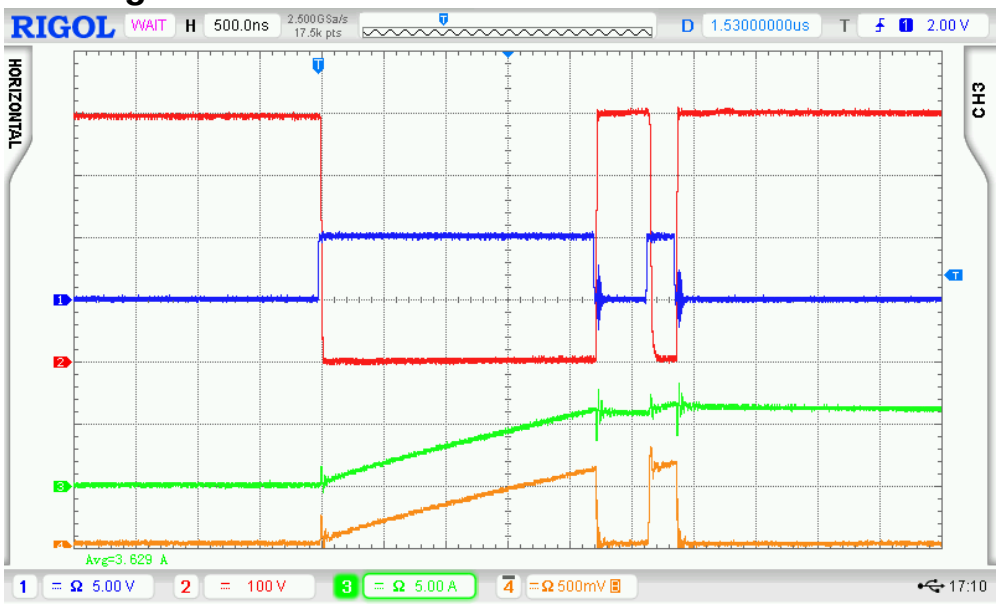

Figure 4-1: Typical Double Pulse Test Waveform captured using DSO. Channel 1(Blue): PWM input (5 V/div); Channel 2(Red): Drain-Source voltage (100 V/div); Channel 3(Green): Inductor Current (5 A/div); Channel 4(Orange): Voltage across 0.1 Ω current sense resistor (500 mV/div); Time scale: 500ns/div

5 Schematic Diagram

The electrical schematic diagram of the TP44200NM-DPT-EVB is shown in Figure 5-1. Various circuit blocks are identified on this diagram to help the user identify or debug the EVB.

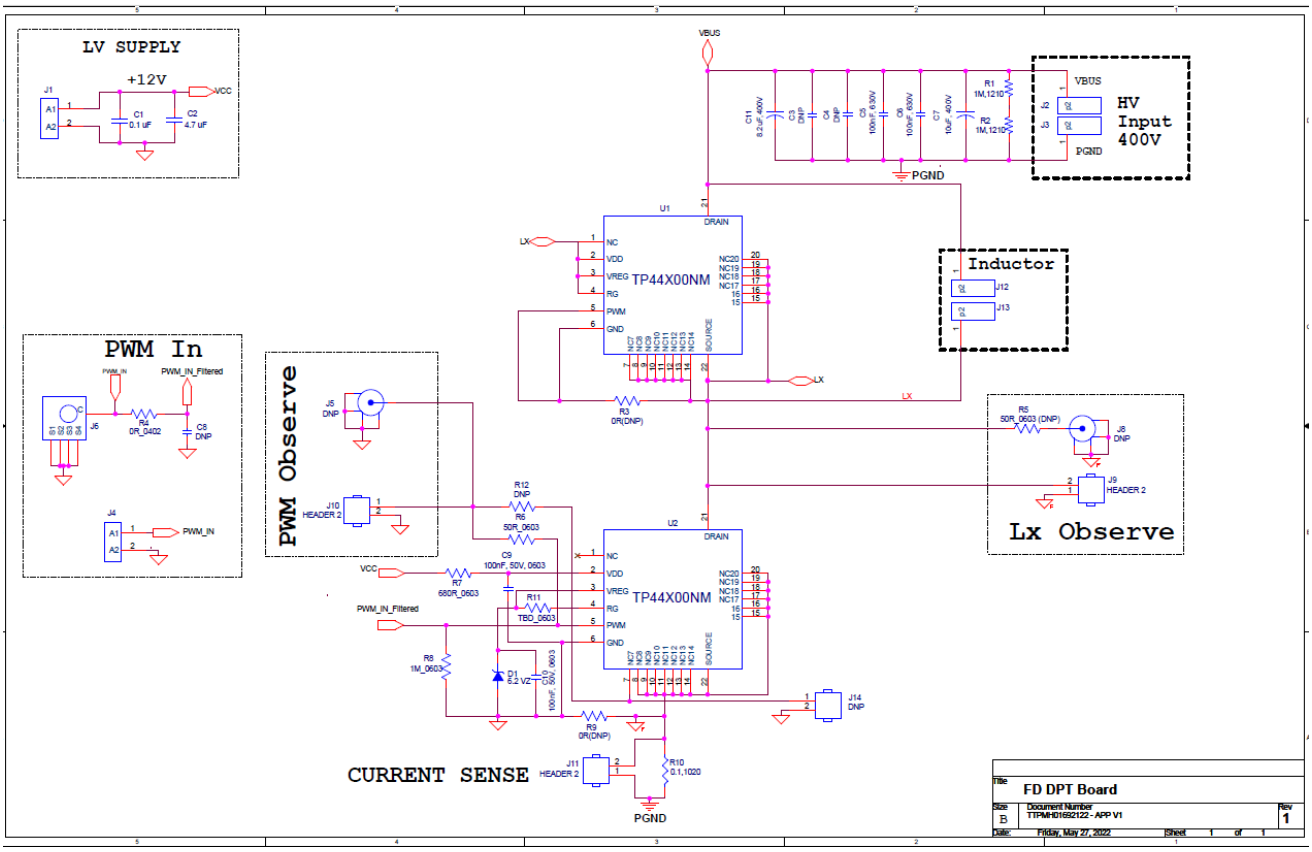

Figure 5-1: Schematic diagram of TP44200NM-DPT-EVB Eval Board.

6 Board Layout

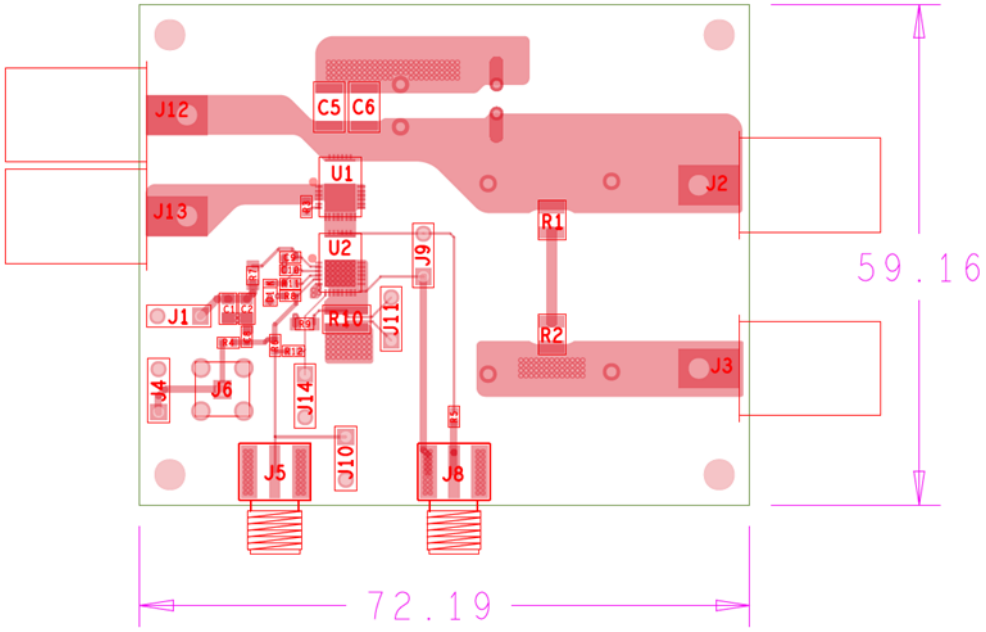

Figure 6-1: EVB PCB Layout of the Top Layer.

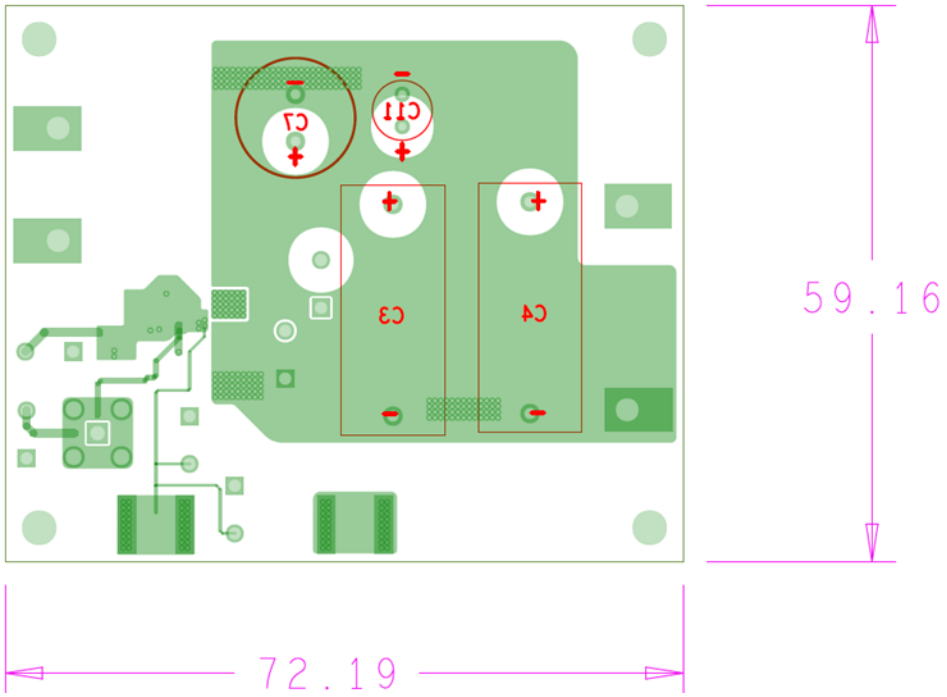

Figure 6-2: EVB PCB Layout of the Bottom Layer.

7 Bill Of Materials

Table 7-1: Bill of Materials (BOM) for TP44200NM-DPT-EVB

TP44200NM-DPT-EVB; BOM Version: 1.1						
Sl. #	**Qty.**	**Ref. Des.**	**Part Description**	**Manufacturer**	**Manufacturer P/N**	**Package**
1	1	C1	DNP			
2	1	C2	4.7uF, 25V, X7R, 0603	Standard	Standard	0603
3	1	C3	DNP			
4	1	C4	DNP			
5	1	C5	100nF, 630V, X7R, 10%	KEMET	C1812C104KDRACAUTO	1812
6	1	C6	100nF, 630V, X7R, 10%	KEMET	C1812C104KDRACAUTO	1812
7	1	C7	ALUM 27uF, 400V, 20%	Standard	Standard	TH
8	1	C8	DNP			
9	1	C9	100nF, 25V, X7R, 0603	Standard	Standard	0603
10	1	C10	100nF, 25V, X7R, 0603	Standard	Standard	0603
11	1	C11	DNP			
12	1	D1	DIODE ZENER 6.2V 300mW SOD323	Onsemi	SZMM3Z6V2ST1G	SOD-323
13	1	J1	HEADER 2 Pin	Standard	Standard	TH
14	1	J4	HEADER 2 Pin	Standard	Standard	TH
15	1	J2	Banana Jack Red 4mm	Standard	Standard	
16	1	J12	Banana Jack Red 4mm	Standard	Standard	
17	1	J3	Banana Jack Black 4mm	Standard	Standard	
18	1	J13	Banana Jack Black 4mm	Standard	Standard	
19	1	J5	DNP			
20	1	J8	DNP			
21	1	J6	SMA Connector	Standard	Standard	TH
22	1	J9	DNP			
23	1	J10	DNP			
24	1	J11	HEADER 2 Pin	Standard	Standard	TH
25	1	J14	DNP			
26	1	R1	RES 1M OHM 5% 1/2W 1210	Standard	Standard	1210
27	1	R2	RES 1M OHM 5% 1/2W 1211	Standard	Standard	1210
28	1	R3	DNP			
29	1	R4	RES 0 OHM JUMPER 1/10W 0603	Standard	Standard	0603
30	1	R5	DNP			
31	1	R6	DNP			
32	1	R7	RES 680 OHM 1% 1/10W 0603	Standard	Standard	0603
33	1	R8	DNP			
34	1	R9	DNP			
35	1	R10	RES 0.100 OHM 1% 1W 1020	Standard	Standard	1020
36	1	R11	RES 20 OHM 1% 1/10W 0603	Standard	Standard	0603
37	1	R12	DNP			
38	1	U1	GaN FET with integrated Driver	Tagore Technology	TP44200NM	QFN 5X7
39	1	U2	GaN FET with integrated Driver	Tagore Technology	TP44200NM	QFN 5X7
40	1		EVB PCB	Tagore Technology	TTPMH01692122 - APP V1	

Revision History

Document version	Date of release	Description of changes
Rev 1.0	25-Nov-2022	First release
Rev 1.1	25-Sep-2023	Revised: EVB Name, Table 2-1, BOM. Font changed.